IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	Unknown	Confirmation No.:	Unknown
First Named Inventor:	Constantin Bulucea	Filing Date:	Herewith
Group Art Unit:	Unknown	Examiner:	Unknown

Division of U.S. parent application 10/054,653 filed 18 January 2002

Atty. Docket No.: NS-5127-1D US

Title: Gate-Enhanced Junction Varactor With Gradual Capacitance Variation

Assignee: National Semiconductor Corporation

Mountain View, California
31 October 2003

MAIL STOP PATENT APPLICATION
COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 CFR 1.56, 1.97, and 1.98, the documents listed on the accompanying substitute PTO Form 1449 are called to the attention of the Examiner for the above patent application. The listed documents include Bulucea, U.S. patent application 09/903,059, filed 10 July 2001. A copy of each of these documents is enclosed. Further enclosed is a copy of an English abstract of each of Japanese Patent Publications 6-61446 and 7-226643. .

All of the preceding documents were cited in U.S. application 09/903,059 or/and in the General Disclosure-of-the-Invention section of the present application.

U.S. application 09/903,059, now pending, was published after the 18 January 2002 filing date of U.S. patent application 10/057,653, the parent of the present application. Application 09/903,059 has the same inventorship as the present application and is assigned to the same assignee as the present application. As far as Applicant's Attorney can determine, application 09/903,059 is not prior art to the present application.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made; or

3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

Please call Applicant's Attorney at 650-964-9797 if you have any questions.

EXPRESS MAIL LABEL NO:

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Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Application No.
	NS-5127-1D US	Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant	Confirmation No.
(Use several sheets if necessary)	Constantin Bulucea	Unknown
	Filing Date	Group
	Herewith	Unknown

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	09/903,059		Bulucea			10 July 2001
	AB	5,399,893	03/95	Weitzel et al.	257	355	
	AC	5,497,028	03/96	Ikeda et al.	257	531	
	AD	6,100,770	08/00	Litwin et al.	331	117 FE	
	AE	6,166,404	12/00	Imoto et al.	257	279	
	AF						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AG	6-61446	03/1994	Japan				X
	AH	7-226643	10/1995	Japan				X

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AH	Andreani, et al., "A 1.8-GHZ CMOS VCO Tuned by an Accumulation-Mode MOS Varactor," IEEE Intl. Symposium on Circuits and Systems, 28 – 31 May 2000, pp. I-315 – I - 318.
	AI	Grove, Physics and Technology of Semiconductor Devices (John Wiley & Sons), 1967, pp. 263 – 305.
	AJ	Grove, et al., "Effect of Surface Fields on the Breakdown Voltage of Planar Silicon *p-n* Junction," IEEE Trans. Electron Devices, vol. ED-14 ,1967, pp. 157 – 162.
	AK	Grove, et al., "Surface Effects on *p-n* Junctions: Characteristics of Surface Space-Charge Regions Under Non-Equilibrium Conditions," Solid-State Electronics, Vol. 9, 1966, pp. 783 - 806.
	AL	Kral, et al., "RF-CMOS Oscillators with Switched Tuning," Procs. IEEE Custom Integrated Circuits Conference, 1998, pp. 555 – 558.
	AM	Lee, The Design of CMOS Radio-Frequency Integrated Circuits (Cambridge Univ. Press), 1998, pp. 37 – 41 and 504 – 514.
	AN	McMahon, et al., "Voltage-Sensitive Semiconductor Capacitors," 1958 IRE Wescon Conf. Rec., Part 3, 19 – 22 August 1958, pp. 72 – 82.
	AO	Moll, "Variable Capacitance With Large Capacity Change," IRE Wescon Conf. Rec., Vol. 3, 1959, pp. 32 - 36.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Application No.
	NS-5127-1D US	10/054,653
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant	Confirmation No.
(Use several sheets if necessary)	Constantin Bulucea	9448
	Filing Date	Group
	January 18, 2002	2814

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AF							
	AG							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AH	Ng, Complete Guide to Semiconductor Devices (McGraw Hill), 1995, pp. 11 - 22.
	AI	Razavi, Design of Analog CMOS Integrated Circuits (McGraw Hill), 2001, pp. 495 – 525.
	AJ	Rusu et al., "Deep-Depletion Breakdown Voltage of Silicon-Dioxide/Silicon MOS Capacitors," IEEE Trans. Elec. Devs., March 1979, pp. 201 - 205.
	AK	Rusu et al., "Reversible Breakdown Voltage Collapse in Silicon Gate-Controlled Diodes," Solid-State Electronics, Vol. 23, 1980, pp. 473 - 480.
	AL	Sedra, et al., Microelectronic Circuits, (4th ed., Oxford Univ. Press), 1998, p. 382.
	AM	Svelto, et al., "A Three Terminal Varactor for RF IC's in Standard CMOS Technology," IEEE Transactions on Electron Devices, Vol. 47, 2000, pp. 893 – 895.
	AN	Warner, Jr., et al., Transistors – Fundamentals for the Integrated-Circuit Engineer (John Wiley & Sons), 1983, pp. 320 – 321.
	AO	Wong et al., "A Wide Tuning Range Gated Varactor," IEEE J. Solid State Circs, May 2000, pp. 773 – 779.

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